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L7: Entry 2 of 19 File: USPT Feb 18, 2003

DOCUMENT-IDENTIFIER: US 6522598 B2
TITLE: Synchronous semiconductor memory device having improved operational frequency margin at data input/output

Brief Summary Text (9):
More specifically, as the storage capacity of the semiconductor memory device increases, the time necessary for testing the device increases and, eventually, the cost for the test and manufacturing cost of the product have been increased.

Brief Summary Text (10):
As a measure to address the increased test time associated with increased storage capacity of the semiconductor memory device, efficiency of testing is improved by testing a plurality of semiconductor memory devices in parallel. The increased storage capacity of the semiconductor memory device mentioned above involves increased number of bits of the address signals to be applied to the semiconductor memory device and multiple bits data input/output interface, and therefore the number of pins for control signals and input/output pins per one semiconductor memory device are increased. Accordingly, the number of semiconductor memory devices which can be tested in parallel at one time is limited.

Brief Summary Text (11):
The number of chips of the semiconductor memory devices which can be measured at one time by a tester is determined by the relation between the number of pins of the tester and the number of pins required by the chip, which relation is generally represented by the following equation.

Brief Summary Text (12):
Further, if the speed of operation of a tester for testing the semiconductor memory device is to be improved along with the improvement of the speed of operation of the semiconductor device, very expensive testing apparatus is necessary, which results in increased cost of testing.

Brief Summary Text (16):
Another object of the present invention is to provide a synchronous semiconductor memory device of which cost of testing is reduced by reducing the number of terminals used for testing so that the number of chips which can be measured simultaneously by one tester is increased.

Brief Summary Paragraph Equation (1):
(Number of pins of the tester)/(number of pins required by the chip)>(number of chips measurable at one time)

Drawing Description Text (34):
FIG. 32 is a schematic block diagram of a structure of scramble circuit 1300 shown in FIG. 29.

Detailed Description Text (17):
Memory array 100 is, as shown in FIG. 2, divided into a total of 16 memory cell blocks 100a to 100p. For example, if synchronous semiconductor memory device 1000 has the storage capacity of 1 G bits, each memory cell block has the capacity of 64 M bits. Each block has such a structure that allows independent operation as a bank.

Detailed Description Text (209):
In the test operation mode, for example, there are provided: a scramble circuit 1300 receiving, among read data corresponding to data input/output terminals DQ0 to DQ3, 4 bits of read data from even-numbered address area and a decode signal from a decoder

1200 for data scrambling; an exclusive OR gate 1302 for performing exclusive OR operation on the data output from scramble circuit 1300; a scramble circuit 1304 for scrambling data in accordance with the data read from odd-numbered address area from the read data corresponding to data input/output terminals DQ0 to DQ3 and to expected value data from decoder 1200; an exclusive OR gate 1306 for outputting data of result of comparison in accordance with the data output from scramble circuit 1304; and a multiplexer circuit 1400 receiving outputs from exclusive OR gate circuit 1302 and 1306 for selectively providing an output to a latch circuit 1148 for an odd-numbered address area and a latch circuit 1146 for even-numbered address, respectively.

Detailed Description Text (210):
The structure corresponding to data input/output terminal DQ1 is basically similar to the structure corresponding to data input/output terminal DQ0 except that latch circuit 1100 is not provided and that scramble circuits 1300 and 1304, exclusive OR gate circuits 1302 and 1306 and multiplexer circuit 1400 which are necessary to output data in the test operation mode are not provided.

Detailed Description Text (214):
Multiplexer circuit 1158 is for distributing, when data from input data latches 1156 and 1154 are to be transmitted internally, the data dependent on whether the address is even-numbered address or odd-numbered address. Multiplexer 1500 provided corresponding to output latches 1146 and 1148 is for providing the data from receivers 1142 and 1144 to a latch preceding an output buffer, dependent on the definition as to whether the data is to be output first or later. Scramble circuit 1324 is a circuit for setting scrambling of data input to the comparator in accordance with input data in a test read cycle, at the time of test read. Multiplexer circuit 1406 is for selectively writing the result of comparison to a latch preceding an output buffer, dependent on whether the result data is to be output first or later.

Detailed Description Text (231):
FIG. 32 is a schematic block diagram showing a structure of scramble circuit 1300 of FIG. 29.

Detailed Description Text (232):
Referring to FIG. 32, scramble circuit 1300 includes exclusive OR gates 1350 to 1356 respectively receiving at one input node, read data RD0 to RD3 from those latch circuits which hold data output at the even-numbered clock edges after CAS latency, among the latch circuits for read data provided corresponding to data input/output terminals DQ0 to DQ3. Exclusive OR gates 1350 to 1356 receive, respectively at the other input gate, decode data DD0 to DD3 output from decoder circuit 1200, respectively.

Detailed Description Text (247):
In the description above, it is assumed that scramble circuit 1300 performs scrambling based on the data applied to 8 data input/output terminals DQ0 to DQ28 at time t11 of FIG. 33. When a structure in which the data applied at time t1 of FIG. 31 is held in a latch circuit or the like is used, it is unnecessary to externally apply data at time point t11.

Detailed Description Text (249):
Further, among 32 pins of data input/output terminals, only 8 pins of data input/output terminals have to be used in the test operation mode. Therefore, it is possible to reduce the total number of input pins and data input/output pins to be controlled by the tester per 1 chip. Therefore, the number of chips which can be tested in parallel simultaneously by the tester apparatus can be increased.

Detailed Description Text (250):
The semiconductor tester for testing the semiconductor devices is expensive, and the cost of testing increases when the number of channeles used increases. By utilizing the test mode of the synchronous semiconductor memory device in accordance with the second embodiment, the number of pins to be used by the semiconductor tester can be reduced. Therefore, for example, it becomes possible to measure two devices simultaneously by one tester, and hence test cost can be reduced.

Detailed Description Text (292):
As to the result of determination of data, 64 bits of data of each cycle are output allocated to 4DQ, the output of result is provided in a period in which the strobe signal QS is at the L level. In this manner, the number of data pins for the output data can be reduced, and the data rate of the output data can be reduced. Therefore, it

becomes possible to monitor outputs by an inexpensive low power tester.

CLAIMS:

2. The synchronous semiconductor memory device according to claim 1, in which build in self test (BIST) is executed in said second mode, wherein said internal circuit includes a memory block; and said data group includes test output data corresponding to command data, address data and storage data for storing operation of said memory block.

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L9: Entry 2 of 9 File: USPT Feb 18, 2003

DOCUMENT-IDENTIFIER: US 6522598 B2
TITLE: Synchronous semiconductor memory device having improved operational frequency margin at data input/output

Brief Summary Text (9):
More specifically, as the storage capacity of the semiconductor memory device increases, the time necessary for testing the device increases and, eventually, the cost for the test and manufacturing cost of the product have been increased.

Brief Summary Text (10):
As a measure to address the increased test time associated with increased storage capacity of the semiconductor memory device, efficiency of testing is improved by testing a plurality of semiconductor memory devices in parallel. The increased storage capacity of the semiconductor memory device mentioned above involves increased number of bits of the address signals to be applied to the semiconductor memory device and multiple bits data input/output interface, and therefore the number of pins for control signals and input/output pins per one semiconductor memory device are increased. Accordingly, the number of semiconductor memory devices which can be tested in parallel at one time is limited.

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Further, if the speed of operation of a tester for testing the semiconductor memory device is to be improved along with the improvement of the speed of operation of the semiconductor device, very expensive testing apparatus is necessary, which results in increased cost of testing.

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Another object of the present invention is to provide a synchronous semiconductor memory device of which cost of testing is reduced by reducing the number of terminals used for testing so that the number of chips which can be measured simultaneously by one tester is increased.

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Memory array 100 is, as shown in FIG. 2, divided into a total of 16 memory cell blocks 100a to 100p. For example, if synchronous semiconductor memory device 1000 has the storage capacity of 1 G bits, each memory cell block has the capacity of 64 M bits. Each block has such a structure that allows independent operation as a bank.

Detailed Description Text (209):
In the test operation mode, for example, there are provided: a scramble circuit 1300 receiving, among read data corresponding to data input/output terminals DQ0 to DQ3, 4 bits of read data from even-numbered address area and a decode signal from a decoder

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Detailed Description Text (210):
The structure corresponding to data input/output terminal DQ1 is basically similar to the structure corresponding to data input/output terminal DQ0 except that latch circuit 1100 is not provided and that scramble circuits 1300 and 1304, exclusive OR gate circuits 1302 and 1306 and multiplexer circuit 1400 which are necessary to output data in the test operation mode are not provided.

Detailed Description Text (214):
Multiplexer circuit 1158 is for distributing, when data from input data latches 1156 and 1154 are to be transmitted internally, the data dependent on whether the address is even-numbered address or odd-numbered address. Multiplexer 1500 provided corresponding to output latches 1146 and 1148 is for providing the data from receivers 1142 and 1144 to a latch preceding an output buffer, dependent on the definition as to whether the data is to be output first or later. Scramble circuit 1324 is a circuit for setting scrambling of data input to the comparator in accordance with input data in a test read cycle, at the time of test read. Multiplexer circuit 1406 is for selectively writing the result of comparison to a latch preceding an output buffer, dependent on whether the result data is to be output first or later.

Detailed Description Text (231):
FIG. 32 is a schematic block diagram showing a structure of scramble circuit 1300 of FIG. 29.

Detailed Description Text (232):
Referring to FIG. 32, scramble circuit 1300 includes exclusive OR gates 1350 to 1356 respectively receiving at one input node, read data RD0 to RD3 from those latch circuits which hold data output at the even-numbered clock edges after CAS latency, among the latch circuits for read data provided corresponding to data input/output terminals DQ0 to DQ3. Exclusive OR gates 1350 to 1356 receive, respectively at the other input gate, decode data DD0 to DD3 output from decoder circuit 1200, respectively.

Detailed Description Text (247):
In the description above, it is assumed that scramble circuit 1300 performs scrambling based on the data applied to 8 data input/output terminals DQ0 to DQ28 at time t11 of FIG. 33. When a structure in which the data applied at time t1 of FIG. 31 is held in a latch circuit or the like is used, it is unnecessary to externally apply data at time point t11.

Detailed Description Text (249):
Further, among 32 pins of data input/output terminals, only 8 pins of data input/output terminals have to be used in the test operation mode. Therefore, it is possible to reduce the total number of input pins and data input/output pins to be controlled by the tester per 1 chip. Therefore, the number of chips which can be tested in parallel simultaneously by the tester apparatus can be increased.

Detailed Description Text (250):
The semiconductor tester for testing the semiconductor devices is expensive, and the cost of testing increases when the number of channeles used increases. By utilizing the test mode of the synchronous semiconductor memory device in accordance with the second embodiment, the number of pins to be used by the semiconductor tester can be reduced. Therefore, for example, it becomes possible to measure two devices simultaneously by one tester, and hence test cost can be reduced.

Detailed Description Text (291):
Referring to FIG. 39, at time t1, internal data information D111 corresponding to active command ACT is output. By using the circuit shown in FIG. 38, it becomes possible to compress and output the data train D11 of FIG. 37 in this manner. Similarly, at time points t2 and t3, data corresponding to commands or the like are

compressed and output. After time point t4, data are also compressed and output in the similar manner, and therefore it is possible to check output data at a data rate one half that of FIG. 37.

Detailed Description Text (292):
As to the result of determination of data, 64 bits of data of each cycle are output allocated to 4DQ, the output of result is provided in a period in which the strobe signal QS is at the L level. In this manner, the number of data pins for the output data can be reduced, and the data rate of the output data can be reduced. Therefore, it becomes possible to monitor outputs by an inexpensive low power tester.

CLAIMS:

2. The synchronous semiconductor memory device according to claim 1, in which build in self test (BIST) is executed in said second mode, wherein said internal circuit includes a memory block; and said data group includes test output data corresponding to command data, address data and storage data for storing operation of said memory block.

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L6: Entry 3 of 10 File: USPT Dec 5, 2000

DOCUMENT-IDENTIFIER: US 6157200 A
TITLE: Integrated circuit device tester

Brief Summary Text (17):
According to the present invention, there is provided an IC device tester which, under the control of a control processor, generates pattern data and expectation data by a pattern generator, formats the pattern data by a formatter into a predetermined pattern waveform, applies the pattern waveform by a driver to an IC device under test at a reference voltage, compares the response signal from the IC device under test by an analog comparator with a reference logical level to make a logical decision, compares the decided logic by a logic comparator with the expectation data from the pattern generator to decide whether or not the IC under test is defective or nondefective, and writes failure data in a failure memory. The IC device tester comprises:

Detailed Description Text (4):
The serial data transceiver 212 outputs and provides various set voltage data, load test conditions, DC test set data, relay matrix control data, etc. to the electro-optic converter 2EO1 and receives via the opto-electric converter 2OE1 DC test result data TX from the test head 100. The formatter 202 formats the test data pattern fed thereto into a predetermined form and provides it to the test head 100 via the electro-optic converter 2EO2. The timing generator 205 applies a timing edge signal to the formatter 202 and generates and sends strobe signals STRB-H and STRB-L to the electro-optic converters 2EO4 and 2EO5, from which they are applied as optical strobe signals to the test head 100. The logic comparator 203 receives the test results (logical data obtained by deciding the results of analog comparison at the strobe timing) from the test head 100 converted by the opto-electric converters 2OE4 and 2OE5 into electric signals, then compares them with expectation data EPD to decide whether or not the IC device under test (hereinafter referred to as a DUT) is nondefective, and write failure data in the failure memory 204.

Detailed Description Text (27):
FIG. 9 illustrates another embodiment of the present invention. In this embodiment the formatter 202 and the logic comparator 203 provided in the tester mainframe 200 in the FIG. 4 embodiment are removed therefrom to the test head 100 to eliminate the need for exchanging the strobe signals between the tester mainframe 200 and the test head 100 and hence reduced the number of optical fibers used correspondingly. Accordingly, pattern data PAD generated by the pattern generator 201 is converted by the electro-optic converter 2EO2 into an optical signal, which is applied via the optical fiber OPF3 to the pin unit 110 of the test head 100, and in a waveform or format controller 130 shown in FIG. 10 the test pattern signal of a real waveform is generated from the pattern data PAD and applied to the DUT. The response signal from the DUT is compared with an expected value in the pin unit 110 and the comparison results (failure data) FDAT are converted into an optical signal, which is sent over the optical fiber OPF7 to the mainframe 200, wherein it is written in the failure memory 204 after being converted by the opto-electric converter 2OE2 into an electric signal.

Detailed Description Text (33):
With the view of generating a pattern signal at the test head side, the pin unit 110 of the test head 100 in this embodiment is provided, as depicted in FIG. 12, with a timing memory 141, a pattern memory 142 and failure memory 143 in association with the format controller 130.

CLAIMS:

1. An integrated circuit device tester which, under the control of a control processor, generates pattern data and expectation data by a pattern generator, formats said

pattern data by a formatter into a predetermined pattern waveform, applies said pattern waveform by a driver to an IC device under test at a reference voltage, compares a response signal from said IC device under test by an analog comparator with a reference logical level to make a logical decision, compares the decided logic by a logic comparator with expectation data from said pattern generator to decide whether or not said IC under test is defective or nondefective, and writes failure data in a failure memory, said IC device tester comprising:

a tester mainframe provided with said control processor;

first serial data transceiver means provided in said tester mainframe, for outputting data, as serial data, which is used to set said reference voltage for said driver and said reference logical level for said analog comparator;

electro-optic converter means provided in said tester mainframe, for converting said serial data to an optical signal;

a test head provided with said driver for applying a test pattern to said IC device under test and an analog comparator for deciding the logic of its response;

opto-electric converter means provided in said test head, for converting said optical signal to serial data of an electric signal;

second serial data transceiver means provided in said test head, for converting said serial data to parallel reference voltage data and parallel reference logical level data;

D/A converter means provided in said test head, for converting said parallel reference voltage data and said parallel reference logical level data to an analog reference voltage and a reference logical level and for setting them in said driver and said analog comparator, respectively; and

optical fiber means for interconnecting said electro-optic converter means and said opto-electric converter means.

9. An integrated circuit device tester which, under the control of a control processor, generates pattern data and expectation data by a pattern generator, formats said pattern data by a formatter into a predetermined pattern waveform, applies said pattern waveform by a driver to an IC device under test at a reference voltage, compares a response signal from said IC device under test by an analog comparator with a reference logical level to make a logical decision, compares the decided logic by a logic comparator with expectation data from said pattern generator to decide whether or not said IC under test is defective or nondefective, and writes failure data in a failure memory, said IC device tester comprising:

a tester mainframe provided with said control processor, said pattern generator, said formatter, said logic comparator and said failure memory;

first electro-optic converter means provided in said tester mainframe, for converting an output test pattern waveform from said formatter to an optical signal;

a test head provided with said driver and said analog comparator;

first opto-electric converter means provided in said test head, for converting a test pattern waveform provided thereto as an optical signal into a test pattern waveform of an electric signal and for applying it to said driver;

second electro-optic converter means provided in said test head, for converting the result of comparison by said analog comparator into an optical signal;

second opto-electric converter means provided in said tester mainframe, for converting said comparison result provided thereto as said optical signal into an electric signal and for applying it to said logic comparator;

first optical fiber means interconnecting the output of said second electro-optic converter means and the input of said first opto-electric converter means, for transmitting a test pattern optical signal from the former to the latter;

second optical fiber means interconnecting the output of said second electro-optic

converter means and the input of said second opto-electric converter means, for transmitting a comparison-result optical signal from the former to the latter;

first serial data transceiver means provided in said tester mainframe, for outputting, as serial data, data for setting said reference voltage for said driver and said reference logical level for said analog comparator;

third electro-optic converter means provided in said tester mainframe, for converting said serial data to an optical signal;

third opto-electric converter means provided in said test head, for converting said optical signal to serial data of an electric signal;

second serial data transceiver means provided in said test head, for receiving said serial data and outputting it as parallel reference voltage data and as parallel reference logical level data;

D/A converter means provided in said test head, for converting said parallel reference voltage data and said parallel reference logical level data to an analog reference voltage and an analog reference logical level and for setting them in said driver and said analog comparator, respectively; and

third optical fiber means interconnecting said third electro-optic converter means and said third opto-electric converter means.

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L10: Entry 27 of 34 File: USPT Nov 28, 2000

DOCUMENT-IDENTIFIER: US 6154862 A
TITLE: Defect analysis memory for memory tester

Brief Summary Text (33):
According to the present invention, there is provided a failure analysis memory for memory testing apparatus wherein: in a test mode for each of steps of testing a memory under stepwise varied test conditions through utilization of test data, an address and expectation data generated by a pattern generator, the test data is written in the memory under test at the said address, data read out therefrom is compared by a logic comparator with the expectation data, and the comparison result is written in the failure analysis memory at the corresponding address to analyze a failure of the memory under test, the failure analysis memory being masked at an address corresponding to that of the memory under test which has failed in the previous test; and in a remove mode, mask data is newly created for the failure analysis memory in preparation for writing therein the comparison result in the next test. The failure analysis memory comprises a failure data storage part and a mask data storage part. The failure data storage part is made up of: a failure data memory having a data input terminal supplied with a predetermined logical level; and a first memory control part which effect control so that, in the test mode, a write enable signal is generated in accordance with the comparison result and the predetermined logical level is written as failure data in the failure data memory at the corresponding address and that, in the remove mode, the failure data is read out from the failure data memory. The mask data storage part is made up of: a mask data memory having a data input terminal supplied with a predetermined logical level; and a second memory control part which effects control so that, in the test mode, mask data is read out of the mask data memory at an address corresponding to the address from the pattern generator and is provided as an inhibit signal to the logic comparator to inhibit it from making a logical comparison at that address and that, in the remove mode, the failure data read out from the failure data memory is applied as a write enable signal to the mask data memory to write therein the logical level as mask data at the corresponding address.

CLAIMS:

1. A failure analysis memory for memory testing apparatus wherein: in a test mode for each of steps of testing a memory under stepwise varied test conditions through utilization of test data, an address and expectation data generated by a pattern generator, said test data is written in said memory under test at said address, data read out therefrom is compared by a logic comparator with said expectation data, the comparison result is written in said failure analysis memory at the corresponding address to analyze a failure of said memory under test, said failure analysis memory being masked at an address corresponding to that of said memory under test that has failed in the previous test; and in a remove mode, mask data is newly created for said failure analysis memory in preparation for writing therein the comparison result in the next test, said failure analysis memory comprising:

a failure data storage part, and

a mask data storage part;

wherein said failure data storage part comprises: a failure data memory having a data input terminal supplied with a predetermined logical level; and a first memory control part which effect control so that, in said test mode, a write enable signal is generated in accordance with said comparison result and said predetermined logical level is written as failure data in said failure data memory at the corresponding address and that, in said remove mode, said failure data is read out from said failure data memory; and

wherein said mask data storage part comprises: a mask data memory having a data input terminal supplied with a predetermined logical level; and a second memory control part which effects control so that, in said test mode, mask data is read out of said mask data memory at an address corresponding to said address from said pattern generator and is provided as an inhibit signal to said logic comparator to inhibit it from making a logical comparison at that address and that, in said remove mode, said failure data read out from said failure data memory is applied as a write enable signal to said mask data memory to write therein said logical level as mask data at the corresponding address.

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L8: Entry 2 of 4 File: USPT Mar 18, 2003

DOCUMENT-IDENTIFIER: US 6536006 B1
TITLE: Event tester architecture for mixed signal testing

Abstract Text (1):
A semiconductor test system having a plurality of different types of tester modules for testing a mixed signal integrated circuit (IC) having analog signals and digital signals with high speed and high efficiency. The semiconductor test system includes two or more tester modules whose performances are different from one another, a test head to accommodate the two or more tester modules, means provided on the test head for electrically connecting the tester modules and a device under test, an optional circuit corresponding to the device under test when the device under test is a mixed signal IC, and a host computer for controlling an overall operation of the test system. Each event tester module includes a tester board which is configured as an event based tester.

Brief Summary Text (2):
This invention relates to a semiconductor test system for testing semiconductor integrated circuits such as a large scale integrated (LSI) circuit, and more particularly, to a semiconductor test system having an event tester architecture which is capable of testing a mixed signal integrated circuit with high speed and high efficiency. In the semiconductor test system of the present invention, a test system is formed by freely combining a plurality of tester modules having identical or different capabilities where each of the tester module operates independently from one another thereby being able to test an analog signal block and a digital signal block of the device under test at the same time.

Brief Summary Text (5):
In the example of FIG. 1, a test processor 11 is a dedicated processor provided within the semiconductor test system for controlling the operation of the test system through a tester bus. Based on pattern data from the test processor 11, a pattern generator 12 provides timing data and waveform data to a timing generator 13 and a wave formatter 14, respectively. A test pattern is produced by the wave formatter 14 with use of the waveform data from the pattern generator 12 and the timing data from the timing generator 13, and the test pattern is supplied to a device under test (DUT) 19 through a driver 15.

Brief Summary Text (6):
A response signal from the DUT 19 resulted from the test pattern is converted to a logic signal by an analog comparator 16 with reference to a predetermined threshold voltage level. The logic signal is compared with expected value data from the pattern generator 12 by a logic comparator 17. The result of the logic comparison is stored in a failure memory 18 corresponding to the address of the DUT 19. The driver 15, the analog comparator 16 and switches (not shown) for changing pins of the device under test, are provided in a pin electronics 20.

Brief Summary Text (11):
In the conventional semiconductor test system, for producing a, test pattern to be applied to a device under test, the test data which is described by, what is called a cycle based format, has been used. In the cycle based format, each variable in the test pattern is defined relative to each test cycle (tester rate) of the semiconductor test system. More specifically, test cycle (tester rate) descriptions, waveform (kinds of waveform, edge timings) descriptions, and vector descriptions in the test data specify the test pattern in a particular test cycle.

Brief Summary Text (16):
An example of devices to be tested includes a type of semiconductor device which has both an analog function and a digital function. A typical example of which is an audio

IC or a communication device IC which includes an analog-digital (AD) converter, a digital-analog (DA) converter and a digital signal processing circuit. In the conventional semiconductor test system, only one type of functional test must be conducted at one time. Therefore, to test the mixed signal integrated circuit noted above, each functional block must be tested separately in a series fashion, such as, first testing the AD converter, then testing the DA converter, and after that, testing the digital signal processing circuit.

Brief Summary Text (22):
In this example, it is assumed that test patterns such as shown by the waveform 31 are to be formed by using such descriptions. The waveforms 31 illustrate test patterns to be generated by pins (tester pins or test channels) Sa and Sb, respectively. The event data describing the waveforms is formed of set edges San, Sbn and their timings (for example, time lengths from a reference point), and reset edges Ran, Rbn and their timings.

Brief Summary Text (23):
For producing a test pattern to be used in the conventional semiconductor test system based on the cycle based concept, the test data must be divided into test cycles (tester rate), waveforms (types of waveforms, and their edge timings), and vectors. An example of such descriptions is shown in the center and left of FIG. 3. In the cycle based test pattern, as shown by waveforms 33 in the left part of FIG. 3, a test pattern is divided into each test cycle (TS1, TS2 and TS3) to define the waveforms and timings (delay time) for each test cycle.

Brief Summary Text (30):
Therefore, it is an object of the present invention to provide a semiconductor test system which has tester modules of different capabilities corresponding to test pins and thus is capable of testing a mixed signal device under test by testing the analog function and the digital function in parallel at the same time.

Brief Summary Text (31):
It is another object of the present invention to provide a semiconductor test system in which tester modules of different pin numbers and capabilities can freely installed in a tester main frame (or test head) and in which specification for connection between the tester modules and the tester main frame is standardized.

Brief Summary Text (32):
It is a further object of the present invention to provide a semiconductor test system which can freely accommodate a plurality of tester modules of different capabilities, thereby testing a plurality of different kinds of devices or functional blocks under test in parallel at the same time.

Brief Summary Text (33):
It is a further object of the present invention to provide a semiconductor test system which can freely accommodate a plurality of tester modules of different capabilities, thereby establishing a test system having a sufficient test performance with low cost, and further enabling to improve its capability in the future.

Brief Summary Text (34):
The semiconductor test system of the present invention includes two or more tester modules whose performances are different from one another, a test head to accommodate the two or more tester modules having different performances, means provided on the test head for electrically connecting the tester modules and a device under test, an optional circuit corresponding to the device under test when the device under test is a mixed signal IC having analog and digital functions, and a host computer for controlling an overall operation of the test system by communicating with the tester modules through a tester bus. One type of the performances of the tester module is a high speed and high timing resolution while other type of performance is a low speed and low timing resolution.

Brief Summary Text (35):
In the semiconductor test system of the present invention, each of the tester modules includes a plurality of event tester boards. Under the control of the host computer, each tester board provides a test pattern to a corresponding pin of the device under test and evaluates a resultant output signal from the device under test.

Brief Summary Text (36):
Since the semiconductor test system of the present invention has a modular structure, a

desired test system can be formed freely depending on the kind of devices to be tested and the purpose of the test. Thus, when the device under test is a mixed signal integrated circuit (having both an analog circuit and a digital circuit therein), the analog circuit and the digital circuit can be tested in parallel at the same time. When the device under test is a high speed logic IC, only a small portion of the logic circuits therein are actually operating in the high speed. Thus, for testing such a high speed logic IC, a small number of tester pins have to have high speed capability. In the semiconductor test system of the present invention, the specification for connecting the test head and tester modules (interface) is standardized. Accordingly, any tester modules having the standard interface can be installed at any positions in the test head.

Brief Summary Text (37):
As noted above, in the semiconductor test system of the present invention, the tester module (tester board) is configured by event based architecture where all the information required for executing the test is prepared in the event based format. Therefore, the rate signal showing the start timing of each test cycle or the pattern generator which operates in synchronism with the rate signal used in the conventional technology are no longer necessary. Because it is not necessary to include the rate signal or pattern generator, each test pin in the event based test system can operate independently from the other test pins. Therefore, different types of test, such as analog circuit test and digital circuit test can be performed at the same time.

Brief Summary Text (38):
Further, because of the event based architecture, the hardware of the event based test system can be dramatically reduced while the software for controlling the tester modules can be dramatically simplified. Accordingly, an overall physical size of the event based test system can be reduced, resulting in further cost reduction, floor space reduction and associated cost savings.

Drawing Description Text (2):
FIG. 1 is a block diagram showing a basic configuration of a semiconductor test system (LSI tester) in the conventional technology.

Drawing Description Text (6):
FIG. 5 is a block diagram showing an example of circuit configuration in an event tester provided in an event tester board which is incorporated in a tester module in accordance with the present invention.

Drawing Description Text (7):
FIG. 6 is a schematic diagram for establishing a semiconductor test system having test pins grouped into different performances by incorporating a plurality of tester modules of the present invention.

Drawing Description Text (8):
FIG. 7 is a block diagram showing an example of tester module which is comprised of a plurality of event tester boards to be used in the semiconductor test system of the present invention.

Detailed Description Text (2):
The embodiment of the present invention is explained with reference to FIGS. 4-10. FIG. 4 is a block diagram showing a basic structure of the semiconductor test system of the, present invention for testing an analog/digital mixed signal integrated circuit (mixed signal IC). In the semiconductor test system of the present invention, a test head (tester main frame) is so configured that one or more modular testers (hereinafter "tester module") are selectively installed therein. The tester modules to be installed can be a plurality of same tester modules depending on the number of tester pins desired or a combination of different tester modules such as a high speed module HSM and a low speed module LSM.

Detailed Description Text (3):
As will be explained with reference to FIGS. 6 and 7 later, each tester module is provided with a plurality of event tester boards 43, for example, eight (8) tester boards. Further, each event tester board includes a plurality of event testers 66 corresponding to a plurality of tester pins, such as 32 event tester for 32 tester pins. Therefore, in the example of FIG. 4, an event tester board 43.sub.1 deals with an analog part of the device test while other event tester boards 43 cover a digital part of the device test.

Detailed Description Text (4):
In the test system of FIG. 4, the plurality of event tester boards 43 are controlled by a tester controller 41, which is a host computer of the test system, through a system bus 64. As noted above, for example, eight event tester boards 43 may be installed in one tester module. Although not shown in FIG. 4, typically, a test system of the present invention is configured by two or more such tester modules as shown in FIG. 6.

Detailed Description Text (5):
In the test system of FIG. 4, the event tester board 43 applies a test pattern (test signal) to a device under test 19, and examines a response signal from the device under test resultant from the test pattern. For testing the analog function of the device under test, an optional circuit 48 may be provided in the test system. Such an optional circuit 48 includes, for example, a DA converter, an AD converter and a filter.

Detailed Description Text (6):
Each event tester board 43 includes event testers 66.sub.1 -66.sub.32 for 32 channels for example, an interface 53, a processor 67 and a memory 68. Each event tester 66 corresponds to a tester pin, and has the same inner structure within the same tester board. In this example, the event tester 66 includes an event memory 60, an event execution unit 47, a driver/comparator 61 and a test result memory 57.

Detailed Description Text (7):
The event memory 60 stores event data for producing a test pattern. The event execution unit 47 produces the test pattern based on the event data from the event memory 60. The test pattern is supplied to the device under test through the driver/comparator 61. In the case where an input pin of the device under test is an analog input, the optional circuit 48 noted above converts the test pattern to an analog signal by the DA converter therein. Thus, the analog test signal is applied to the device under test. An output signal of the device under test is compared with an expected signal by the driver/comparator 61, the result of which is stored in the test result memory 57. In the case where an output signal from the device under test is an analog signal, if necessary, such an analog signal is converted to a digital signal by the AD converter in the optional circuit 48.

Detailed Description Text (8):
FIG. 5 is a block diagram showing an example of configuration in the event tester 66 in the event tester board 43 in more detail. The further detailed description regarding the event based test system is given in the above U.S. patent application as well as U.S. patent application Ser. No. 09/259,401 owned by the same assignee of this invention. In FIG. 5, the blocks identical to that of FIG. 4 are denoted by the same reference labels.

Detailed Description Text (9):
The interface 53 and the processor 67 are connected to the tester processor (host computer) 41 through the system bus 64. The interface 53 is used, for example, for transferring data from the tester controller 41 to a register (not shown) in the event tester board to assign the event testers to the input/output pins of the device under test. For example, when the host computer sends a group assigning address to the system bus, the interface 53 interprets the group assigning address and allows the data from the host computer to be stored in the register in the specified event tester board.

Detailed Description Text (10):
The processor 67 is provided, for example, in each event tester board, and controls the operations in the event tester board including generation of events (test patterns), evaluation of output signals from the device under test, and acquisition of failure data. The processor 67 can be provided at each tester board or every several tester boards. Further, the processor 67 may not always necessary be provided in the event tester board, but the same control functions can be made directly by the tester controller 41 to the event tester boards.

Detailed Description Text (15):
In the event tester summarized above, the input signal applied to the device under test and the expected signal compared with the output signal of the device under test are produced by the data in the event based format. In the event based format, the information of change points on the input signal and expected signal is formed of action information (set and/or reset) and time information (time length from a specified point).

Detailed Description Text (19):

FIG. 6 is a schematic diagram for establishing a semiconductor test system having test pins grouped into different performances by incorporating a plurality of tester modules of the present invention.

Detailed Description Text (20):
A test head 124 is provided with a plurality of tester modules depending on, for example, the number of pins of a test fixture 127, a type of the device to be tested, and the number of pins of the device to be tested. As will be described later, an interface (connection) specification between the test fixture and the test module is standardized so that any tester modules can be installed in any positions in the test head.

Detailed Description Text (21):
The test fixture 127 includes a large number of elastic connectors such as pogo-pins to electrically and mechanically connect the tester modules and a performance board 128. The device under test 19 is inserted in a test socket on the performance board 128, thereby establishing an electrical communication with the semiconductor test system. The optional circuit 48 shown in FIG. 4 to be used in analog testing can be formed on the performance board 128 depending on the specification of the device to be tested.

Detailed Description Text (22):
Each of the tester module has a predetermined number of pin groups. For example, one high speed module HSM installs printed circuit boards corresponding to 128 test pins (test channels) while one low speed module LSM installs printed circuit boards corresponding to 256 test pins. These numbers are disclosed only for an exemplary purpose, and various other numbers of test pins are also possible. In the example of FIG. 7, the tester module is configured by 256 channels as a basic unit in which eight (8) event tester boards 43 are installed. Each event tester board includes, for example, 32 event testers (test channels) .

Detailed Description Text (23):
As noted above, each board in the tester module has event testers each of which generates and applies test patterns to the corresponding pin of the device under test through the performance board 128. Output signals of the device under test 19 responsive to the test pattern are transmitted to the event tester board in the tester module through the performance board 128 and are compared with the expected signals to determine the pass/fail of the device under test.

Detailed Description Text (24):
Each tester module is provided with an interface (connector) 126. The connector 126 is so arranged to fit to the standard specification of the test fixture 127. For example, in the standard specification of the test fixture 127, a structure of connector pins, impedance of the pins, distance between the pins (pin pitch), and relative positions of the pins are specified for the intended test head. By using the interface (connector) 126 which matches the standard specification on all of the tester modules, test systems of various combinations of the tester modules can be freely established.

Detailed Description Text (26):
FIG. 8 is a block diagram showing a basic concept for conducting different types of test in parallel for a mixed signal device 19 having analog and digital functions by the semiconductor test system of the present invention. In this example, the mixed signal device 19 includes an AD converter circuit, a logic circuit, and a DA converter circuit. The semiconductor test system of the present invention can perform test for each group of specified number of tester pins independently from the other group as noted above. Therefore, by assigning the groups of tester pins to these circuits in the mixed signal device, these circuits can be tested in parallel at the same time.

Detailed Description Text (28):
In contrast, when testing the mixed signal IC shown in FIG. 8 by the semiconductor test system of the present invention, the AD converter circuit, logic circuit and DA converter circuit can be tested in parallel at the same time as shown in FIG. 9B. Thus, the present invention can dramatically reduce the overall test time. Since it is a common practice to evaluate the test result of the AD converter circuit or DA converter circuit by predetermined formulas, a computation time after each of the AD and DA circuit test is provided in FIGS. 9A and 9B.

Detailed Description Text (30):
The event based test system of the present invention does not need the pattern generator and the timing generator used in the conventional semiconductor test system

configured by the cycle based concept. Therefore, it is possible to substantially decrease the physical size of the overall test system by installing all of the modular event testers in the test head (or tester main frame) 124.

Detailed Description Text (32):
As noted above, in the semiconductor test system of the present invention, the tester module (tester board) is configured by event based architecture where all the information required for executing the test is prepared in the event based format. Therefore, the rate signal showing the start timing of each test cycle or the pattern generator which operates in synchronism with the rate signal used in the conventional technology are no longer necessary. Because it is not necessary to include the rate signal or pattern generator, each test pin in the event based test system can operate independently from the other test pins. Therefore, different types of test, such as analog circuit test and digital circuit test can be performed at the same time.

Detailed Description Text (33):
Since the semiconductor test system of the present invention has a modular structure, a desired test system can be formed freely depending on the kind of devices to be tested and the purpose of the test. Further, the hardware of the event based test system can be dramatically reduced while the software for the test system can be dramatically simplified. Accordingly, the tester modules of different capabilities and performances can be installed together in the same test system. Furthermore, as shown in FIG. 6, an overall physical size of the event based test system can be considerably reduced, resulting in further cost reduction, floor space reduction and associated cost savings.

CLAIMS:

1. A semiconductor test system for testing a mixed signal integrated circuit, comprising: two or more tester modules whose performances are different from one another where each tester module includes at least one event tester which produces a test pattern based on test data described in an event format; a test head to accommodate the two or more tester modules having different performances; means provided on the test head for electrically connecting the tester modules and a device under test; an optional circuit corresponding to the device under test when the device under test is a mixed signal integrated circuit having an analog function block and a digital function block, and a host computer for controlling an overall operation of the test system by communicating with the tester modules through a tester bus; whereby the analog function block and the digital function block of the mixed signal integrated circuit being tested in parallel at the same time, and wherein the event data defines events as any changes in the test pattern generated by the event tester at timings relative to one fixed reference point.

2. A semiconductor test system for testing a mixed signal integrated circuit as defined in claim 1, wherein one type of the performances of the tester module is a high speed and high timing resolution while another type of performance is a low speed and low timing resolution.

3. A semiconductor test system for testing a mixed signal integrated circuit as defined in claim 1, wherein interface specification for connecting the tester modules and the means for electrically connecting the tester modules and the device under test is standardized.

4. A semiconductor test system for testing a mixed signal integrated circuit as defined in claim 1, wherein the means for electrically connecting the tester modules and the device under test is comprised of a performance board having a test socket for mounting the device under test thereon and signal patterns connected to the test socket, and a test fixture having a connection mechanism for electrically connecting between the performance board and the tester modules,thereby establishing electrical communication between the device under test and the tester modules.

5. A semiconductor test system for testing a mixed signal integrated circuit as defined in claim 1, wherein a number of tester pins for each tester module is variable.

6. A semiconductor test system for testing a mixed signal integrated circuit as defined in claim 1, wherein a number of tester pins is variably assigned to the tester module, and such assignment of test pins and modification thereof are regulated by address data from the host computer.

7. A semiconductor test system for testing a mixed signal integrated circuit as defined in claim 1, wherein each of the tester modules includes a plurality of event tester boards where each of the event tester boards includes a plurality of event testers which are assigned to a predetermined number of test pins.

8. A semiconductor test system for testing a mixed signal integrated circuit as defined in claim 7, wherein each of the tester modules corresponds to one of the event tester boards.

9. A semiconductor test system for testing a mixed signal integrated circuit as defined in claim 7, wherein each of the tester modules includes a plurality of event tester boards wherein each of the event tester boards includes an inner controller where the inner controller controls, in response to instructions from the host computer, to generate a test pattern, supply the test pattern to the device under test, and to evaluate an output signal of the device under test.

10. A semiconductor test system for testing a mixed signal integrated circuit as defined in claim 1, wherein each of the tester modules includes an inner controller where the inner controller controls, in response to instructions from the host computer, to generate a test pattern from the tester module, supply the test pattern to the device under test, and to evaluate an output signal of the device under test.

11. A semiconductor test system for testing a mixed signal integrated circuit as defined in claim 1, wherein each of the tester modules includes a plurality of event tester boards each having a plurality of event tester where each of the event testers is assigned to one test pin, wherein each event tester is comprised of: a controller which controls, in response to instructions from the host computer, an operation of the event tester; an event memory for storing timing data for each event; an address sequencer for providing, under the control of the controller, address data to the event memory; means for producing the test pattern based on the timing data from the event memory; and a driver/comparator for transferring the test pattern to a corresponding pin of the device under test and receiving the output signal from the device under test.

WEST

End of Result Set

Generate Collection Print

L8: Entry 4 of 4 File: USPT Dec 18, 2001

DOCUMENT-IDENTIFIER: US 6331770 B1
TITLE: Application specific event based semiconductor test system

Abstract Text (1):
A semiconductor test system for testing semiconductor devices, and particularly, to a semiconductor test system having a plurality of different types of tester modules in a main frame and a measurement module unique to the device under test in a test fixture, thereby achieving a low cost and application specific test system. The semiconductor test system includes two or more tester modules whose performances are different from one another, a test system main frame to accommodate a combination of two or more tester modules, a test fixture provided on the main frame for electrically connecting the tester modules and a device under test, a measurement module provided in the test fixture for converting signals between the device under test and the tester module depending on the function of the device under test, and a host computer for controlling an overall operation of the test system by communicating with the tester modules through a tester bus.

Brief Summary Text (2):
This invention relates to a semiconductor test system for testing semiconductor integrated circuits such as a large scale integrated (LSI) circuit, and more particularly, to a low cost semiconductor test system configured exclusively to a specific application and has an event based tester architecture. The event based semiconductor test system of the present invention is formed by freely combining a plurality of tester modules having identical or different capabilities and a measurement module specific to an intended application where each of the tester module operates independently from one another, thereby establishing a low cost test system. The measurement module may be installed in a test fixture of the test system.

Brief Summary Text (4):
FIG. 1 is a schematic block diagram showing an example of a semiconductor test system, also called an IC tester, in the conventional technology for testing a semiconductor integrated circuit (hereafter may also be referred to as "device under test").

Brief Summary Text (5):
In the example of FIG. 1, a test processor 11 is a dedicated processor provided within the semiconductor test system for controlling the operation of the test system through a tester bus. Based on pattern data from the test processor 11, a pattern generator 12 provides timing data and waveform data to a timing generator 13 and a wave formatter 14, respectively. A test pattern is produced by the wave formatter 14 with use of the waveform data from the pattern generator 12 and the timing data from the timing generator 13, and the test pattern is supplied to a device under test (DUT) 19 through a driver 15.

Brief Summary Text (6):
A response output signal from the DUT 19 is produced in response to the test pattern. The output signal is converted to a logic signal by an analog comparator 16 with reference to a predetermined threshold voltage level. The logic signal is compared with expected value data from the pattern generator 12 by a logic comparator 17. The result of the logic comparison is stored in a failure memory 18 corresponding to the address of the DUT 19. The driver 15, the analog comparator 16 and switches (not shown) for changing pins of the device under test, are provided in a pin electronics 20.

Brief Summary Text (11):
In the conventional semiconductor test system, for producing a test pattern to be

applied to a device under test, the test data which is described by, what is called a cycle based format, has been used. In the cycle based format, each variable in the test pattern is defined relative to each test cycle (tester rate) of the semiconductor test system. More specifically, test cycle (tester rate) descriptions, waveform (kinds of waveform, edge timings) descriptions, and vector descriptions in the test data specify the test pattern in a particular test cycle.

Brief Summary Text (16):
An example of devices to be tested includes a type of semiconductor device which has both an analog function and a digital function. A typical example of which is an audio IC or a communication device IC which includes an analog-digital (AD) converter, a digital-analog (DA) converter and a digital signal processing circuit. Further, there is a type of semiconductor device which has a functionality for testing an inner circuit by itself, i.e., built-in self-test (BIST).

Brief Summary Text (17):
In the conventional semiconductor test system, it is constituted so that only one type of functional test can be conducted at one time. Therefore, to test the mixed signal integrated circuit noted above, each functional block must be tested separately in a series fashion, such as, first testing the AD converter, then testing the DA converter, and after that, testing the digital signal processing circuit. Further, in testing the device having the BIST function, such a test for evaluating the BIST function must be carried out separately from the other types of test.

Brief Summary Text (23):
In this example, it is assumed that test patterns such as shown by the waveforms 31 are to be formed by using such descriptions. The waveforms 31 illustrate test patterns to be generated at pins (tester pins or test channels) Sa and Sb, respectively. The event data describing the waveforms is formed of set edges San, Sbn and their timings (for example, time lengths from a reference point), and reset edges Ran, Rbn and their timings.

Brief Summary Text (24):
For producing a test pattern to be used in the conventional semiconductor test system based on the cycle based concept, the test data must be divided into test cycles (tester rate), waveforms (types of waveforms, and their edge timings), and vectors. An example of such descriptions is shown in the center and left of FIG. 3. In the cycle based test pattern, as shown by waveforms 33 in the left part of FIG. 3, a test pattern is divided into each test cycle (TS1, TS2 and TS3) to define the waveforms and timings (delay times) for each test cycle.

Brief Summary Text (31):
Therefore, it is an object of the present invention to provide a semiconductor test system which is dedicated to a specific application by having tester modules of different capabilities corresponding to test pins and a measurement module to be used for the specific application in a test fixture.

Brief Summary Text (32):
It is another object of the present invention to provide a low cost semiconductor test system which is capable of testing a semiconductor device having an analog function and a digital function by testing the analog and digital functions in parallel at the same time by incorporating tester modules of different capabilities corresponding to test pins and an analog measurement module in a test fixture.

Brief Summary Text (33):
It is a further object of the present invention to provide a low cost semiconductor test system which is capable of testing a semiconductor device having a BIST (built-in self-test) function and other logic function by testing the BIST and logic functions in parallel at the same time by incorporating tester modules of different capabilities corresponding to test pins and a BIST measurement module in a test fixture.

Brief Summary Text (34):
It is a further object of the present invention to provide a semiconductor test system having tester modules of different capabilities corresponding to test pins wherein interface specification between the test system main frame and the tester modules is standardized for freely accommodating tester modules of different pin counts and performances in the main frame.

Brief Summary Text (35):

It is a further object of the present invention to provide a semiconductor test system which can freely accommodate a plurality of tester modules of different capabilities, thereby being able to carry out tests on a plurality of different kinds of devices or functional blocks at the same time.

Brief Summary Text (37):
The semiconductor test system of the present invention includes two or more tester modules whose performances are different from one another, a test system main frame for installing two or more tester modules therein, a test fixture provided on the test system main frame for electrically connecting the tester modules and a device under test, a measurement module provided in the test fixture for converting signals between the tester modules and the device under test depending on an intended function of the device under test, and a host computer for controlling an overall operation of the test system by communicating with the tester modules through a tester bus.

Brief Summary Text (38):
In the semiconductor test system of the present invention, a measurement module unique to the test application is provided in the test fixture which established electrical connection between the tester modules and the device under test. The test fixture will be replaced depending on the test object. Each of the tester modules includes a plurality of event tester boards. Under the control of the host computer, each tester board provides a test pattern to a corresponding pin of the device under test and evaluates a resultant output signal from the device under test.

Brief Summary Text (41):
As noted above, in the semiconductor test system of the present invention, the tester module (tester board) is configured by event based architecture where all the information required for executing the test is prepared in the event based format. Because it is not necessary to include the rate signal or pattern generator, each test pin in the event based test system can operate independently from the other test pins. Therefore, different types of test, such as analog circuit test and digital circuit test can be performed at the same time.

Brief Summary Text (42):
Further, since the test system of the present invention is configured with a modular basis, a simple and low cost test system can be established depending on the type of test deice or test purpose. Furthermore, because of the event based architecture, the hardware of the event based test system can be dramatically reduced while the software for controlling the tester modules can be dramatically simplified. Accordingly, an overall physical size of the event based test system can be reduced, resulting in further cost reduction, floor space reduction and associated cost savings.

Drawing Description Text (2):
FIG. 1 is a block diagram showing a basic configuration of a semiconductor test system (LSI tester) in the conventional technology.

Drawing Description Text (6):
FIG. 5 is a block diagram showing an example of circuit configuration in an event tester provided in an event tester board which is incorporated in a tester module in accordance with the present invention.

Drawing Description Text (7):
FIG. 6 is a schematic diagram for establishing a semiconductor test system having test pins grouped into different performances by incorporating a plurality of tester modules of the present invention.

Detailed Description Text (3):
In the semiconductor test system of the present invention, a test head (tester main frame) is so configured that one or more modular testers (hereinafter "tester modules") are selectively installed therein. The tester modules to be installed can be a plurality of same tester modules depending on the number of tester pins desired or a combination of different tester modules such as a high speed module HSM and a low speed module LSM.

Detailed Description Text (4):
As will be explained with reference to FIGS. 6 and 7 later, each tester module is provided with a plurality of event tester boards 43, for example, eight (8) tester boards. Further, each event tester board includes a plurality of event testers 66 corresponding to a plurality of tester pins, such as 32 event testers for 32 tester

pins. Therefore, in the example of FIG. 4, an event tester board 43.sub.1 deals with an analog part of the device test while other event tester boards 43 cover a digital part of the device test.

Detailed Description Text (5):
In the test system of FIG. 4, the plurality of event tester boards 43 are controlled by a tester controller 41, which is a host computer of the test system, through a system bus 64. As noted above, for example, eight event tester boards 43 may be installed in one tester module. Although not shown in FIG. 4, typically, a test system of the present invention is configured by two or more such tester modules as shown in FIG. 6.

Detailed Description Text (6):
In the test system of FIG. 4, the event tester board 43 applies a test pattern (test signal) to a device under test 19, and examines a response signal from the device under test resulted from the test pattern. For testing the analog function of the device under test, an analog measurement (test) module 48 may be provided in the test system. Such an analog measurement module 48 includes, for example, a DA converter, an AD converter and a filter. As will be described later, the analog measurement module 48 is installed in a test fixture (pin fixture) of the test system.

Detailed Description Text (7):
Each event tester board 43 includes event testers 66.sub.1 -66.sub.32 for 32 channels for example, an interface 53, a processor 67 and a memory 68. Each event tester 66 corresponds to a tester pin, and has the same inner structure as that of the other within the same tester board. In this example, the event tester 66 includes an event memory 60, an event execution unit 47, a driver/comparator 61 and a test result memory 57.

Detailed Description Text (8):
The event memory 60 stores event data for producing a test pattern. The event execution unit 47 produces the test pattern based on the event data from the event memory 60. The test pattern is supplied to the device under test 19 through the driver/comparator 61. In the case where an input pin of the device under test 19 is an analog input, the analog measurement module 48 noted above converts the test pattern to an analog signal by the DA converter therein. Thus, the analog test signal is applied to the device under test 19. An output signal of the device under test 19 is compared with an expected signal by the driver/comparator 61, the result of which is stored in the test result memory 57. In the case where an output signal from the device under test 19 is an analog signal, if necessary, such an analog signal is converted to a digital signal by the AD converter in the analog measurement module 48.

Detailed Description Text (9):
FIG. 5 is a block diagram showing an example of configuration in the event tester 66 in the event tester board 43 in more detail. The further detailed description regarding the event based test system is given in the above U.S. patent application Ser. No. 09/406,300 as well as U.S. patent application Ser. No. 09/259,401 owned by the same assignee of this invention. In FIG. 5, the blocks identical to that of FIG. 4 are denoted by the same reference labels.

Detailed Description Text (10):
The interface 53 and the processor 67 are connected to the tester processor (host computer) 41 through the system bus 64. The interface 53 is used, for example, for transferring data from the tester controller 41 to a register (not shown) in the event tester board to assign the event tester to the input/output pins of the device under test. For example, when the host computer 41 sends a group assigning address to the system bus 64, the interface 53 interprets the group assigning address and allows the data from the host computer to be stored in the register in the specified event tester board.

Detailed Description Text (11):
The processor 67 is provided, for example, in each event tester board, and controls the operations in the event tester board including generation of events (test patterns), evaluation of output signals from the device under test, and acquisition of failure data. The processor 67 can be provided at each tester board or every several tester boards. Further, the processor 67 may not always necessary be provided in the event tester board, but the same control functions can be made directly by the tester controller 41 to the event tester boards.

Detailed Description Text (16):

In the event tester summarized above, the input signal applied to the device under test and the expected signal compared with the output signal of the device under test are produced by the data in the event based format. In the event based format, the information of change points on the input signal and expected signal is formed of action information (set and/or reset) and time information (time length from a specified point).

Detailed Description Text (20):
FIG. 6 is a schematic diagram for establishing a semiconductor test system having test pins grouped into different performances by incorporating a plurality of tester modules of the present invention.

Detailed Description Text (21):
A test head 124 is provided with a plurality of tester modules depending on, for example, the number of pins of a test fixture 127 connected to the test head, a type of device to be tested, and the number of pins of the device to be tested. As will be described later, an interface (connection) specification between the test fixture 127 and the test module is standardized so that any tester modules can be installed in any positions in the test head (system main frame).

Detailed Description Text (22):
The test fixture 127 includes a large number of elastic connectors such as pogo-pins to electrically and mechanically connect the tester modules and a performance board 128. The device under test 19 is inserted in a test socket on the performance board 128, thereby establishing an electrical communication with the semiconductor test system. Although not shown in FIG. 6 but is shown in FIGS. 7A and 7B, in the present invention, measurement modules specific to the test (such as analog measurement module 48) are installed in the test fixture 127. Therefore, the test fixture 127 in the present invention is designed unique to the specific test application.

Detailed Description Text (24):
Each of the tester module 125 has a predetermined number of pin groups. For example, one high speed module HSM installs printed circuit boards corresponding to 128 test pins (test channels) while one low speed module LSM installs printed circuit boards corresponding to 256 test pins. These numbers are disclosed only for an illustration purpose, and various other numbers of test pins are also possible.

Detailed Description Text (25):
As noted above, each printed circuit board in the tester module has event testers which generates test patterns and applies the same to the corresponding pin of the device under test 19 through the performance board 128. Output signals of the device under test 19 responsive to the test pattern are transmitted to the event tester board in the tester module through the performance board 128 whereby being compared with the expected signals to determine the pass/fail of the device under test.

Detailed Description Text (26):
Each tester module is provided with an interface (connector) 126. The connector 126 is so arranged to fit to the standard specification of the test fixture 127. For example, in the standard specification of the test fixture 127, a structure of connector pins, impedance of the pins, distance between the pins (pin pitch), and relative positions of the pins are specified for the intended test head. By using the interface (connector) 126 which matches the standard specification on all of the tester modules, test systems of various combinations of the tester modules can be freely established.

Detailed Description Text (28):
FIG. 7A is a block diagram showing an example of semiconductor test system configured for testing a mixed signal device, and FIG. 7B is a block diagram showing an example of semiconductor test system configured for testing a BIST function device. For simplicity of illustration, the interface 126 in FIG. 6 is not shown here. Further, the tester modules 125 are simply denoted by TM, although each of which may be same or different from one another depending on the purpose of the test.

Detailed Description Text (29):
The semiconductor test system of FIG. 7A is so configured that it is dedicated to a device under test which has an analog circuit therein. Accordingly, analog measurement (test) modules 132 and 133 are provided in the test fixture 127. For example, when a particular input pin of the device under test is an analog signal pin, a test signal from the tester module 125 is converted to an analog signal by the analog measurement (test) module 133 having a DA converter. Thus, the analog test signal is applied to the

particular input pin of the device under test. Further, when a particular output pin of the device under test is an analog signal pin, the output signal from the output pin is converted to a digital signal by the analog measurement (test) module 132 having an AD converter. Thus, the digital output signal is transmitted to the tester module 125.

Detailed Description Text (30):
As in the foregoing, the application of the test fixture in the test system of the present invention is limited to a specific test object. Accordingly, the tester modules 125 can be completely separated from the analog functions and be designed to deal with only digital signals. Thus, overall cost of the test system can be substantially decreased. Moreover, an interface structure between the tester modules and the test fixtures is simplified.

Detailed Description Text (34):
FIG. 8 is a block diagram showing a basic concept for conducting different types of test in parallel for a mixed signal device 19 having analog and digital functions by the semiconductor test system of the present invention. In this example, the mixed signal device 19 includes an AD converter circuit, a logic circuit, and a DA converter circuit. The semiconductor test system of the present invention can perform test for each group of specified number of tester pins independently from the other group as noted above. Therefore, by assigning the groups of tester pins to these circuits in the mixed signal device, these circuits can be tested in parallel at the same time.

Detailed Description Text (36):
In contrast, when testing the mixed signal IC shown in FIG. 8 by the semiconductor test system of the present invention, the AD converter circuit, logic circuit and DA converter circuit can be tested in parallel at the same time as shown in FIG. 9B. Thus, the present invention can dramatically reduce the overall test time. Since it is a common practice to evaluate the test result of the AD converter circuit or DA converter circuit by predetermined formulas, a computation time after each of the AD and DA circuit test is provided in FIGS. 9A and 9B.

Detailed Description Text (38):
The event based test system of the present invention does not need the pattern generator and the timing generator used in the conventional semiconductor test system configured by the cycle based concept. Therefore, it is possible to substantially decrease the physical size of the overall test system by installing all of the modular event testers in the test head (or tester main frame) 124.

Detailed Description Text (39):
As has been foregoing, in the event based test system of the present invention, the test fixture (pin fixture) installs the measurement (test) modules designed for specific applications, thereby simplifying the tester modules to be inserted in the test system. Accordingly, by replacing the test fixtures prepared based on the specific applications, it is easily able to establish a semiconductor test system of simple and low cost.

Detailed Description Text (41):
As noted above, in the semiconductor test system of the present invention, the tester module (tester board) is configured by event based architecture where all the information required for executing the test is prepared in the event based format. Therefore, different types of test, such as analog circuit test and digital circuit test can be performed at the same time.

Detailed Description Text (42):
Since the semiconductor test system of the present invention has a modular structure, a desired test system can be formed freely depending on the kind of devices to be tested and the purpose of the test. Further, the hardware of the event based test system can be dramatically reduced while the software for the test system can be dramatically simplified. Accordingly, the tester modules of different capabilities and performances can be installed together in the same test system. Furthermore, as shown in FIG. 6, an overall physical size of the event based test system can be considerably reduced, resulting in further cost reduction, floor space reduction and associated cost savings.

CLAIMS:

1. A semiconductor test system, comprising:

two or more tester modules whose performances are identical to or different from one another;

a test system main frame for accommodating an arbitrary combination of the tester modules therein;

a test fixture provided on the test system main frame for electrically connecting the tester modules and a device under test;

a measurement module provided in the test fixture for converting signals between the device under test and the tester module depending on a function of the device under test; and

a host computer for controlling an- overall operation of the test system by communicating with the tester modules in the test system through a tester bus.

5. A semiconductor test system as defined in claim 1, wherein specification for connecting the test fixture and the tester module is standardized.

6. A semiconductor test system as defined in claim 1, wherein the test fixture includes a performance board having a mechanism for mounting the device under test thereon and a connection mechanism for electrically connecting between the performance board and the tester modules.

7. A semiconductor test system as defined in claim 1, wherein a number of tester pins is variably assigned to the tester module.

8. A semiconductor test system as defined in claim 1, wherein a number of tester pins is variably assigned to the tester module, and such assignment of test pins and modification thereof are regulated by address data from the host computer.

9. A semiconductor test system as defined in claim 1, wherein each of the tester modules includes a plurality of event tester boards where each of the event tester boards is assigned to a predetermined number of test pins.

10. A semiconductor test system as defined in claim 1, wherein each of the tester modules includes an inner controller where the inner controller controls, in response to instructions from the host computer, to generate a test pattern from the tester module and to evaluate an output signal of the device under test.

11. A semiconductor test system as defined in claim 9, wherein each of the tester modules includes a plurality of event tester boards wherein each of the event tester boards includes an inner controller where the inner controller controls, in response to instructions from the host computer, to generate a test pattern from the tester module and to evaluate an output signal of the device under test.

12. A semiconductor test system as defined in claim 1, wherein each of the tester modules includes a plurality of event tester boards where each of the event tester boards is assigned to one test pin, wherein each of the event tester boards is comprised of:

a controller which controls, in response to instructions from the host computer, to generate the test pattern from the tester module and to evaluate an output signal of the device under test;

an event memory for storing timing data for each event;

an address sequencer for providing, under the control of the controller, address data to the event memory;

means for producing a test pattern based on the timing data from the event memory; and

a driver/comparator for transferring the test pattern to a corresponding pin of the device under test and receiving a response output signal from the device under test.

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DOCUMENT-IDENTIFIER: US 5610925 A
TITLE: Failure analyzer for semiconductor tester

Abstract Text (1):
A failure analyzer for the semiconductor tester which tests a plurality of devices at the same time and stores a first fail information for each device under test (DUT) and inhibits further fail information from being stored in a fail memory. The failure analyzer includes a plurality of comparators connected to corresponding DUT for generating a fail signal when the output signal from the DUT disagrees with an expected signal, a fail memory connected to the comparators to store fail information on the DUT, a plurality of fail receiving circuits for receiving the fail signals from the comparators wherein each of the fail receiving circuits counts the number of the fail signal from corresponding one of the comparators and generating a counted signal when the fail signal reaches a predetermined number, a plurality of inhibit circuits connected to the fail receiving circuits to inhibit the fail signals received after the predetermined number from affecting the fail memory, an OR-gate for combining output signals from the inhibit circuits to generate an overall fail signal, and a fail memory controller connected to the fail memory to enable the fail memory when receiving the overall fail signal from the OR-gate.

Brief Summary Text (2):
The present invention relates to a failure analyzer for a semiconductor tester, and more particularly, to a failure analyzer which can memorize the first failure information of each of a plural devices under simultaneous measurement.

Brief Summary Text (4):
Generally, most failure analyzers for a semiconductor tester have only one control part for failure analysis. For this reason, in a plural-device test, it was hard to detect the failure position of all devices at once.

Brief Summary Text (8):
Regarding a difference between their capacity, in fact, there is possibility that all test patterns are used for a single-device failure analysis. However, such a small capacity has been suppose to be enough for the failure memory.

Brief Summary Text (14):
It is a purpose of this present invention to provide a failure analyzer for a semiconductor tester, so as to improve the above mentioned problem existing in the conventional technique, and more particularly, to provide a failure analyzer which can analyze plural devices with one cycle of test pattern and store their failure data; namely, to provide a failure analyzer which is available for plural-device simultaneous measurement.

Detailed Description Text (7):
The present invention are comprised of the above description and brings about the following effect; in a plural-device simultaneous measurement, the present invention enables the failure analyzer for the semiconductor tester to memorize the failure information of each DUT with one cycle of test pattern, without failure analyzers which are equivalent to the number of devices to be tested.

CLAIMS:

1. A failure analyzer for a semiconductor tester for simultaneously measuring a plurality of semiconductor devices, comprising:

a plurality of comparators connected to corresponding semiconductor devices to be

tested (DUT) to receive output signals from said semiconductor devices, each of said comparators generating a fail signal when the output signal from said DUT disagrees with an expected signal;

a fail memory connected to outputs of said plurality of comparators to store fail information of said DUT;

a plurality of fail receiving circuits for receiving said fail signals from said comparators, each of said fail receiving circuits counting the number of said fail signal from corresponding one of said comparators and generating a counted signal when the number of said fail signal reaches a predetermined value;

a plurality of inhibit circuits connected to said fail receiving circuits to inhibit said fail signals received after said counted signal from affecting said fail memory; and

an OR-gate for combining output signals from said plurality of inhibit circuits to generate an overall fail signal; and

a fail memory controller connected to said fail memory and said OR-gate to enable said fail memory when receiving said overall fail signal from said OR-gate.